

CLAIMS

What is claimed is:

- 1 1. A computer system comprising:
 - 2 a memory; and
 - 3 a memory controller, wherein the memory controller includes a refresh
 - 4 timing circuit for generating clock pulses used to trigger memory refresh
 - 5 events.
- 1 2. The computer system of claim 1, wherein the refresh timing circuit triggers
 - 2 memory refresh events whenever the computer system is operating in a normal mode
 - 3 and a low power mode.
- 1 3. The computer system of claim 2, wherein the refresh timing circuit further
 - 2 comprises:
 - 3 a clock generator for generating the clock pulses;
 - 4 a first counter coupled to the clock generator;
 - 5 a storage register coupled to the clock generator and the counter; and
 - 6 a comparator coupled to the clock generator, the counter and the
 - 7 storage register.

1 4. The computer system of claim 3, wherein the first counter counts the number
2 of clock pulses generated by the clock generator.

1 5. The computer system of claim 4, wherein the first counter transmits data to the
2 storage register whenever the computer system is operating in the normal mode, the
3 data representing the number of clock pulses counted by the counter since the
4 occurrence of a prior memory refresh event.

1 6. The computer system of claim 5, wherein the storage register transmits the
2 data to the comparator upon a transition from the normal mode to the low power
3 mode.

1 7. The computer system of claim 6, wherein the first counter transmits signals to
2 the comparator whenever the computer system is operating in the low power mode,
3 the signal representing the number of clock pulses received from the clock generator.

1 8. The computer system of claim 7, wherein the comparator compares the signal
2 received from the first counter and the data received from the storage register, and
3 wherein the comparator transmits a refresh trigger signal whenever there is a match
4 between the signal and the data.

1 9. The computer system of claim 4, wherein the refresh timing circuit further
2 comprises a second counter.

1 10. The computer system of claim 9, wherein the first counter counts the number
2 of clock pulses generated by the clock generator while the computer system is
3 operating in the low power mode and the second counter counts the number of clock
4 pulses generated by the clock generator while the computer system is operating in a
5 normal mode.

1 11. The computer system of claim 10, wherein the second counter transmits data
2 to the storage register upon the occurrence of a memory refresh event whenever the
3 computer system is operating in the normal mode, the data representing the number of
4 clock pulses counted by the counter since the occurrence of a previous memory
5 refresh event.

1 12. The computer system of claim 11, wherein the second counter is deactivated
2 and the first counter is activated whenever the computer system transitions from the
3 normal mode to the low power mode.

1 13. The computer system of claim 12, wherein the first counter transmits signals
2 to the comparator whenever the computer system is operating in the low power mode,
3 the signal representing the number of clock pulses received from the clock generator.

1 14. The computer system of claim 3, wherein the refresh timing circuit includes a
2 second counter for triggering memory refresh events whenever the computer system is
3 operating in the normal mode

1 15. The computer system of claim 1, wherein the memory is an Extended Data
2 Out Dynamic Random Access Memory (EDO DRAM) and the memory controller is
3 an EDO DRAM controller.

1 16. An Extended Data Out Dynamic Random Access Memory (EDO DRAM)
2 controller comprising:
3 a refresh timing circuit for generating clock pulses used to trigger
4 memory refresh events.

1 17. The computer system of claim 16, wherein the refresh timing circuit further
2 comprises:
3 a clock generator;
4 a first counter coupled to the clock generator;

5 a storage register coupled to the clock generator and the counter; and
6 a comparator coupled to the clock generator, the counter and the
7 storage register.

1 18. The EDO DRAM controller of claim 17, wherein the EDO DRAM controller
2 operates in a normal mode and a low power mode.

1 19. The EDO DRAM controller of claim 18, wherein the first counter counts the
2 number of clock pulses generated by the clock generator.

1 20. The EDO DRAM controller of claim 19, wherein the first counter transmits
2 data to the storage register whenever the EDO DRAM controller is operating in the
3 normal mode, the data representing the number of clock pulses counted by the counter
4 since the occurrence of a previous memory refresh event.

1 21. The EDO DRAM controller of claim 20, wherein the storage register transmits
2 the data to the comparator upon a transition from the normal mode to the low power
3 mode.

1 22. The EDO DRAM controller of claim 21, wherein the first counter transmits
2 signals to the comparator whenever the EDO DRAM controller is operating in the

3 low power mode, the signal representing the number of clock pulses received from
4 the clock generator.

1 23. The EDO DRAM controller of claim 22, wherein the comparator compares
2 the signal received from the first counter and the data received from the storage
3 register, and wherein the comparator transmits a refresh trigger signal whenever there
4 is a match between the signal and the data.

1 24. The EDO DRAM controller of claim 19, wherein the refresh timing circuit
2 further comprises a second counter.

1 25. The EDO DRAM controller of claim 24, wherein the first counter counts the
2 number of clock pulses generated by the clock generator while the EDO DRAM
3 controller is operating in the low power mode and the second counter counts the
4 number of clock pulses generated by the clock generator while the EDO DRAM
5 controller is operating in the normal mode.

1 26. The EDO DRAM controller of claim 25, wherein the second counter transmits
2 data to the storage register upon the occurrence of a memory refresh event whenever
3 the EDO DRAM controller is operating in the normal mode, the data representing the

4 number of clock pulses counted by the counter since the occurrence of a previous
5 memory refresh event.

1 27. The EDO DRAM controller of claim 26, wherein the second counter is
2 deactivated and the first counter is activated whenever the EDO DRAM controller
3 transitions from the normal mode to the low power mode.

1 28. The EDO DRAM controller of claim 27, wherein the first counter transmits
2 signals to the comparator whenever the EDO DRAM controller is operating in the
3 low power mode, the signal representing the number of clock pulses received from
4 the clock generator.

1 29. A method of calibrating a refresh timer in a computer system, the method
2 comprising:
3 counting a first set of clock pulses received at a counter from a clock
4 generator;
5 receiving a signal indicating that a memory refresh event has been
6 triggered; and
7 storing a first count representing the number of clock cycles received
8 at the counter before receiving the signal.

1 30. The method of claim 29, further comprising:
2 resetting the counter after storing the first count;
3 counting a second set of clock pulses;
4 receiving the signal indicating that a memory refresh event has been
5 triggered; and
6 storing a second count.

1 31. The method of claim 29, wherein the refresh timer is a low power mode
2 refresh timer.

1 32. In a computer system having a normal mode of operation and a low power
2 mode of operation, a method of triggering a memory refresh event while the computer
3 system is operating in the low power mode, the method comprising:
4 transmitting a frequency value to a comparator, the frequency value
5 representing the frequency at which to trigger memory refresh events;
6 transmitting a first clock pulse count to the comparator;
7 determining whether the first clock pulse count is equal to the
8 frequency value; and
9 transmitting a first refresh signal.

1 33. The method of claim 32, further comprising:

2 transmitting a second clock pulse count to the comparator if it is
3 determined that the first clock pulse is not equal to the frequency value;
4 determining whether the second clock pulse count is equal to the
5 frequency value; and
6 transmitting the first refresh signal.

1 34. The method of claim 32, further comprising transitioning from the normal
2 mode of operation to the low power mode of operation before transmitting the
3 frequency value to the comparator.

1 35. The method of claim 32, wherein the process of transmitting the first clock
2 pulse count to the comparator further comprises:
3 transmitting a clock pulse from a clock generator to a counter;
4 incrementing the counter; and
5 transmitting the incremented count to the comparator.

1 36. The method of claim 35, further comprising resetting the counter before
2 transmitting the clock pulse from the clock generator.

1 37. The method of claim 35, further comprising:
2 resetting the counter after transmitting the refresh signal;

~~transmitting a second clock pulse to the second clock input of the first counter; determining whether the second clock pulse is received by the second counter; determining a frequency value; and transmitting a second refresh signal to the second counter.~~[illegible]